Remarks

Acceptance/formal entry therefor of this preliminarily submitted amendment prior to the Examiner taking up the above-identified application for a formal review is respectfully requested.

The continuing data information on page 1 of the Specification has been updated, accordingly.

By the amendments presented hereinabove, originally submitted claims 1-8 are being substituted with newly presented claims 9-27.

The claims feature schemes for testing the operating condition of the wafer chip areas (i.e., while the chips are in wafer-state) such as during a burn-in testing which judges electrical connection/non-connection such as between a test needle connected to a test apparatus at burn-in and a terminal of the chip area/chip. The three claim groups, i.e., claims 9-12, claims 13-15 and claims 16-22, are directed to a semiconductor wafer or a semiconductor chip and are adapted for testing the operational condition of the chip(s). For example, the invention according to claim 9 calls for a semiconductor wafer including chip areas in which each contains a memory matrix, first and second terminals and a further terminal, with the first terminal being coupled to receive a signal for judging electrical connection/non-connection between a needle connected to a test apparatus at burn-in and the further terminal provided in the respective chip area and, moreover, the second terminal is for outputting a response signal in accordance with the signal applied to the first terminal. According to independent claim 13, the invention calls for a semiconductor wafer including chip areas in which each contains a memory matrix including memory cells, which may be of the volatile or nonvolatile type, address input terminals for

receiving an address signal to specify a memory cell in the matrix, data input/output terminals, control signal terminals for receiving control signals to control the write and read operations of the memory matrix and test-only signal terminals for inputting signals to judge the electrical connection condition between a needle connected to a test apparatus at burn-in and a terminal provided in each of the chip areas. According to independent claim 16, the invention calls for a semiconductor chip including a memory circuit with a memory matrix, a terminal and a test circuit with regard to judging the electric connection condition between a needle connected to a test apparatus at burn-in and the terminal of the semiconductor chip and providing a response signal for responding to the signal received by the test circuit and on the basis of this judging the electric connection/non-connection between the needle connected to the test apparatus at the burn-in and the terminal of the semiconductor. The test circuit according to claims 16+ includes a test clock terminal, first and second test control terminals, a test (I/O) terminal and first and second power terminals.

According to the invention in claims 16+, Figs. 1-2, as combined with, for example, Fig. 6, are related thereto. For example, the semiconductor wafer 32 in Fig. 6 is shown to include plural semiconductor chips/chip areas 31 which contain the memory matrix such as the SRAM 1 and the test circuit 2 of Figs. 1-2. As can be seen from the Fig. 2 illustration of the test circuit contained within the chip/chip area, there is included a test clock terminal, first and second test control terminals CTRL1 and CTRL 2, a test I/O terminal which is provided with a command/test input data and power terminals applied with power source Vcc and ground potential Vss. Such is also applicable with regard to the invention according to claim groups including claims 9+ and 13+. In that regard,

see also the Fig. 20 example embodiment regarding a testing system which adds the test apparatus to functions for outputting the output enable signals "/OE" as it relates to each of the chip areas/chips of the wafer.

The invention according to newly presented claims 23-26 is directed to a manufacturing scheme for a semiconductor device containing one or more semiconductor chips from two manufactured semiconductor wafers. The method calls for producing a first semiconductor wafer including first semiconductor chips and a second semiconductor wafer including second semiconductor chips, performing burn-in of the first and second wafers, cutting (i.e., dicing) the first and second semiconductor wafers to produce separate batches of first and second semiconductor chips and assembling one or more of the first semiconductor chips and one or more of the second semiconductor chips to produce the device (e.g., packaged device). With regard to performing burn-in testing of the two wafers, claim 24 (dependent on claim 23) calls for performing a contact check for judging electric connection/non-connection between each needle connected to a test apparatus and each terminal provided in each of the first and second semiconductor chips within the first and second semiconductor wafers. An example of this is given with regard to Fig. 8 of the drawings in which the burn-in process is shown in the example illustration of Fig. 7 of the drawings, although the invention is not necessarily limited thereto.

Although featured aspects which are contained in the present substitute claims may also be contained with regard to the claims in the U.S. Patent corresponding to the prior, parent application (listed on page 1 of the Specification), a clear line of demarcation between the present claimed subject matter and that disclosed by the claims of applicants' prior patent exists.

Examination and favorable action therefor of the present, substitute claims is respectfully requested.

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Respectfully submitted,
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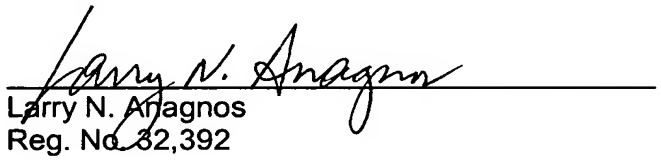

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